A HYBRID MULTI-POINT SIGNAL AVERAGER

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In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

By

Y. PARAMESWAR

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August 7,1979

(P.R.K. RAO)
Professor
Department of Electrical Engineering
Indian Institute of Technology
Kanpur

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This thesis has been approved for the award of the degree of Master of Technology (M. Tech) in accordance with the regulations of the Indian Institute of Technology Kanpur
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CONTENTS

ABSTRACT

In many areas of science and engineering signal averagers are used to extract signals heavily masked by noise. Signal averagers employing analog techniques suffer from a serious drawback of poor retentivity. On the other hand the resolutions obtainable with digital signal averagers is limited by the speed of the analog to digital converters used and the delays involved in memory access. To overcome these difficulties a hybrid signal averaging scheme is proposed in this thesis. The scheme employs charge transfer device (CTD) as a time-base expander followed by a digital processor for achieving high resolution and signal-to-noise enhancement. Resolutions of the order of 100 nsec can be obtained using this technique in a cost effective way. This thesis report gives in detail the system design and description of such a hybrid scheme.

CHAPTER 1

INTRODUCTION

In many areas of scientific research and engineering analysis, the signal appearing at the output of detectors used in measurement, monitoring or analysis systems is contaminated appreciably by noise and sometimes even burried in noise, making even the detectability of the desired signal a difficult task. In such situations, one common method of attenuating noise is to limit the bandwidth of the monitoring instruments by conventional filtering. If the instrument bandwidth is wider than the desired signal's bandwidth, the extra bandwidth only admits extra noise and can be discarded without losing any of the signal. Conventional filtering is of little value when the signal and noise occupy the same part of the frequency spectrum.

If the signal to be detected is of a known shape the correlation techniques may be used to improve the signal-to-noise ratio. In those cases where the signal is unknown but repetitive, an enhancement of the signal-to-noise ratio can be carried out by making use of the technique of ensemble averaging (time averaging) or signal averaging as it is often termed. This technique uses an averaging or integration procedure similar to that employed when multiple recorder or oscilloscope traces are superimposed to obtain an average or effective value.

Basically, signal averaging involves the instrumental superposition of a number of signal traces by sampling each signal record in the same way and storing the samples in either a digital or analog register. Because the records are each sampled in the same way and at the same corresponding times, the signals add coherently in register while the noise being rancom averages to zero. Averaging the ensemble of records thus provides increased signal-to-noise ratio (SNR). This technique of time averaging may easily be seen to yield an improvement in signal-to-noise ratio equal to the square root of the number of repetitions of the signal.

1.1 HIGH RESOLUTION WITH HYBRID TECHNIQUE

As described above, in the case of repetitive signals, an enhancement in the signal-to-noise ratio can be carried out by making use of an averaging technique and the instruments implementing the technique are generally called signal averagers which may be analog, digital or hybrid in nature depending on the signal processing circuitry employed.

Signal averagers demand only that some means be available for synchronizing them to the repetitive signal that is to be pulled out of the noise. Generally this synchronizing signal or trigger pulse, can be derived from the signal or can be used to initiate the signal record. The synchronizing signal must be reliable in predicting the start of the signal for the records to add exactly and for S/N enhancement to be realized.

Most of the schemes employed for time averaging a signal or waveform for SNR enhancement, are based on the correlation techniques [2], in which the signal samples are correlated with synchronous rectangular pulses of fixed duration over a time slot.

Depending upon whether averaging is carried out at a single point on the waveform or at a number of points simultaneously, on a single repetition of the waveform, we realize single channel (single point) or multi-point operation. Multi-channel operation evidently has a higher time-efficiency.

With the use of special purpose digital instruments more convenient and more precise enhancement of noisy repetitive signals can be obtained. In these instruments, the time resolution (spacing between two points) is mainly restricted by the speed of the analog to digital converter used. Even if the high speed A/D converters are available, the resolution cannot be increased because of the time delays involved in the memory-access and other digital circuits.

Recent advances in the charge-transfer device LSI technology have lead to the availability of discrete time analog signal processing devices [9,13,15]. These devices function in the discrete-time domain by storing samples of the input signal in analog memory as packets of charge.

There are two basic categories of devices based on the way in which the analog samples are handled. In the charge transfer devices (CTD) each sample of charge is transferred from stage to stage across the chip under a sequence of clock pulses. The second category is single transfer devices (STD). These devices are similar to an integrated set of multiplexed sample and holds. Each successive sample is stored in a separate discrete memory cell, where it stays until it is read-out.

The repetition rates and duty cycles of the waveforms which the signal averagers are called upon to process are rather low. In such situations, a hybrid system in which analog signal can be sampled at a high speed and processed digitally at lower speeds is an attractive solution.

This thesis describes, one such hybrid signal averaging system in which analog and digital storage systems are used for achieving high resolution and long memory retention.

1.2 ORGANIZATION OF THE REPORT

This report is divided into five chapters for convenience. In Chapter 2, signal averaging concepts are discussed in brief. In the same chapter, a section is devoted for charge transfer devices (CTD) and how CTD's can be used for high speed transient analog storage.

System specifications and design are presented in Chapter 3. System hardware description is presented in Chapter 4. Conclusions and suggestions for further improvements are reported in Chapter 5.

CHAPTER 2

SOME AVERAGING TECHNIQUES

In this chapter, signal averagers using analog techniques and digital techniques are discussed, considering their merits and demerits. In the last section a hybrid scheme of signal averaging is presented.

2.1 SIGNAL AVERAGING USING ANALOG TECHNIQUES

2.1.1 Boxcar Integrator:

Analog gated integration of a small portion of a synchronously repetitive noisy waveforms or of a number of equal time slots of the waveforms simultaneously is capable of providing very high SNR enhancement. This scheme applies only to repetitive waveforms which occur in synchronism with a pilot trigger or a synchronizing pulse. The pilot trigger is used to control the analog transmission gate opening on the time scale, so that the same portion of the waveform could be considered over the integration period, on each repetition of the waveform.

An analog method of single-channel averaging uses the boxcar integrator shown in Fig. 2.1. In the Boxcar integrator [12], the analog gate (or sampling gate) can be opened on a selected time during the passage of the signal to be measured. At a fixed delay, the gate is synchronized to the signal through the reference channel, so that the same portion of the signal is sampled for each signal passage. The gated samples taken from each passage are

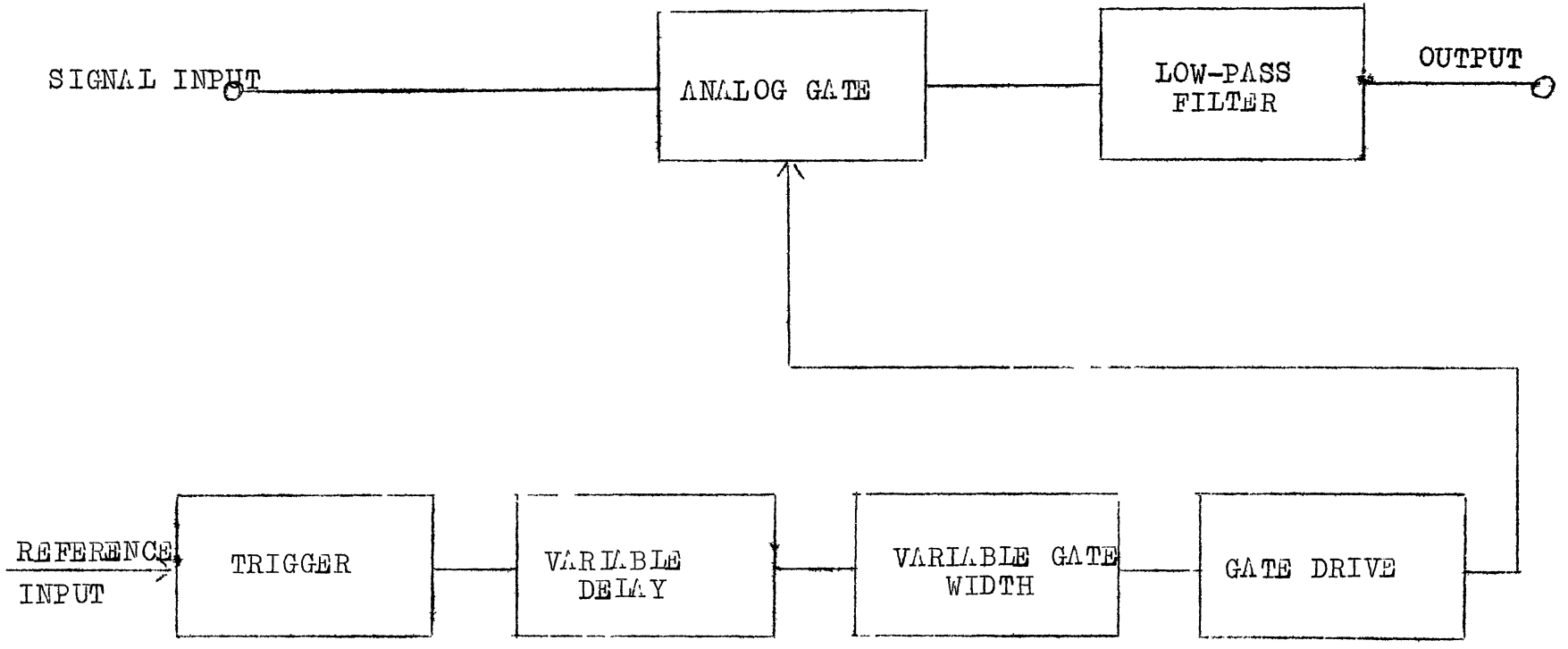

FIG. 2.1 SCHEMATIC BLOCK DIAGRAM OF A BOXCAR INTEGRATOR.

then averaged by the low-pass (RC) filter to provide signal-to-noise enhancement for the portion of the signal which is sampled.

The signal-to-noise improvement ratio depends on the apertur time (the time for which gate is open) and on the time constant of the low-pass filter. The effective time constant of the low-pass filter can be increased by using an Op-Amp integrater as a low-pass filter.

After N repetitions of the waveform, when the output has fully responded to the input, it can be shown [12], that this process leads to a signal to noise improvement ratio (SNIR) of the portion of width AT corresponding to the time delay τ from the trigger detection instant and the SNIR is given by

$$\text{SNIR} = \sqrt{\left(\frac{2 \times \text{Time constant}}{\text{Aperture time}}\right)} = \sqrt{\left(\frac{2 \times TC}{AT}\right)} \qquad (2.1)$$

where TC = Time constant of the low-pass filter = RC

AT = Aperture time

The SNIR given by Eq.(2.1) is realized only when an effective averaging time equal to atleast five times the time constant for each slot on the waveform.

The delay τ can be fixed, incremented in steps or continuously increased at a rate consistent with the above considerations for the recovery of the complete waveform.

Compared to a multi-point averager, to be discussed in Section 2.1.2, the boxcar integrator is a rather inefficient instrument for enhancing complex signals. Because the signal is sampled only briefly for each of its appearances, a great deal of information is thrown away. In fact, for a signal averager having n channels, signal enhancement will proceed n times faster than for a boxcar integrator with similar gate characteristics. Because the boxcar integrator has only a single channel (gate), the gate can be made far more sophisticated than would be practical for the large number of channels in the multi-point signal averager. Hence the boxcar integrator is most useful in applications involving fast signals.

2.1.2 Multi-point Gated-Analog Integrators:

A multi-point gated analog integrator can be visualized as a string of boxcar averagers, the sampling gates of which are opened sequentially in time. At precisely the selected moment, the first gate opens for a selected period of time. When it closes, the next gate opens and so on until all of the gates have been opened. This process is repeated for the number of repetitions required to produce the required signal-to-noise ratio improvement. By sequentially observing the output of each boxcar averager, it is possible to obtain a view of the entire waveform or some selected portion of it.

A multi-point averager operates in exactly this manner. It contains n independent memories, each of which is sequentially exposed to a small segment of the input waveform. The output is obtained by sequentially reading out the memories [10]6]

Multi-point averagers have the advantage of recovering the entire waveform in the shortest possible time when compared to boxcar integrator. But the resolution obtained in a multi-point averager is much less compared to boxcar integrator.

Multi-point analog-gated integrators do not provide as many time increments as digital signal averagers, and then for longer time duration waveforms will not have the resolution of the digital signal averagers. Because of their low retention time for their memory storage, analog signal averagers are inferior to digital signal averagers.

2.2 DIGITAL SIGNAL AVERAGERS

Signal averagers sample input signals at fixed time intervals, convert the samples to digital form, and store the sample values at separate locations in a memory. The sampling theorem tells that no information is lost by this discrete representation, provided that the sampling rate is atleast twice as fast as the highest frequency present in the input signal.

The sampling process is continued for a preset number of repetitions of the desired signal. During the first repetition, sample values are stored in memory, with each memory location corresponding to a definite sample value. Then, during subsequent repetitions, the new sample values are added algebraically to the values accumulated at the corresponding memory locations. After any given number of repetitions, the sum stored in each memory location is equal to the number of repetitions times the average of the samples taken at the point on the desired waveform.

This simple summation process tends to enhance the signal with respect to the noise. The signal portion of the input is a constant for any sample point, so its contribution to the stored sum is multiplied by the number of repetitions. On the other hand, the random noise makes both positive and negative contributions at any sample point during successive repetitions. Therefore, the noise portion of the stored sum grows more slowly than the signal portion.

The averaging or summation process can be described as follows. Let the input be f(t), composed of a repetitive signal portion s(t) and a noise portion n(t). Say, the kth repetition of s(t) begins at time t_k (and let $t_1 = 0$). Finally, let samples be taken every T seconds. We have then

$$f(t) = s(t) + n(t) \qquad (2.2)$$

The signal is sampled, and the sample values are

$$f(t_k + iT) = s(t_k + iT) + n(t_k+iT)$$

$$= s(iT) + n(t_k+iT) \qquad (2.3)$$

Two assumptions will now be made which are valid for most noise situations, namely,

1. That the mean value of the noise is zero.
2. That the variance of the noise, σ_n^2 is constant over the period of the record.

Under these conditions the r.m.s. value of the noise will be equal to the square root of the variance and we can write the signal/noise voltage ratio of the ith sample as:

$$S/N = \frac{s(iT)}{\sigma} \qquad (2.4)$$

After M repetitions, the value stored at the ith memory location is

$$\sum_{k=1}^{M} f(t_k+iT) = \sum_{k=1}^{M} s(iT) + \sum_{k=1}^{M} n(t_k+iT)$$

$$= M\, s(iT) + \sum_{k=1}^{M} n(t_k + iT) \qquad (2.5)$$

Since the noise is random and the m samples are independent, the mean square value of the sum of the M noise samples is $M\sigma^2$, and the r.m.s. value in $\sqrt{M}\,\sigma$. Therefore the signal-to-noise ratio after summation is

$$(S/N)_M = \frac{Ms(iT)}{\sqrt{M}\,\sigma} = \sqrt{M}\,(S/N) \qquad (2.6)$$

Thus the summation of M repetitions of the noisy signal will result in a $\sqrt{M}$ improvement in the signal/noise ratio.

2.2.1 Averaging in the Frequency Domain:

The methods till now discussed consider the separation of a signal from a noisy waveform in terms of the time domain. Often the unwanted waveform is periodic and can be at a frequency quite close to that of the desired signal. In such cases the methods of signal averaging are still valid provided that the unwanted signal is not harmonically related to the desired signal.

If we consider s(t) to be periodic with a period τ, then the summation of M repetitions of the waveform is equivalent to the convolution of the input signal $f(t) = s(t) + n(t)$ with a train of M unit pulses, that is, with the sync. pulse train.

Convolving the input f(t) with M unit pulses spaced τ seconds apart gives

$$a(t) = \int_{-\infty}^{\infty} f(t - \xi) \sum_{k=1}^{M} \delta(\xi - k\tau)\,d\xi$$

$$= \sum_{k=1}^{M} f(t - k\tau) \qquad (2.7)$$

This represents the output of averaging system in the time domain. Its corresponding characteristics in the frequency

domain can be derived from the translation of the impulse response of the system which is clearly:

$$h(t) = \sum_{k=1}^{M} \delta(t - k\tau) \qquad (2.8)$$

The transfer function of the averager $H(j\omega)$,

$$\left|H(j\omega)\right| = \left|\frac{\sin\left(\frac{\omega m\tau}{2}\right)}{\sin\left(\frac{\omega\tau}{2}\right)}\right| \qquad (2.9)$$

The function given by Eq.(2.9) is repeated over the frequency range for each discrete value of t, resulting in the comb filter shown in Fig.2.2.

The longer the signal to be filtered then the narrower will be the effective transfer function expressed in the frequency domain. Since the required signal, f(t), is time synchronized with the repetition frequency then every frequency component of f(t) coincides with the centre of one of the teeth of the comb filter. Consequently as M increases, the bandwidth of the filter is reduced and the signal-to-noise ratio is improved. As the value of M becomes greater the phase relationship between the signal and synchronizing pulse becomes more important. Unless this is kept constant as M is increased the effective bandwidth of the comb teeth will widen and deteriorate the action of the signal averager.

2.2.2 Averaging Techniques:

The basic summation process described in the Section 2.2 has the disadvantage that during the averaging

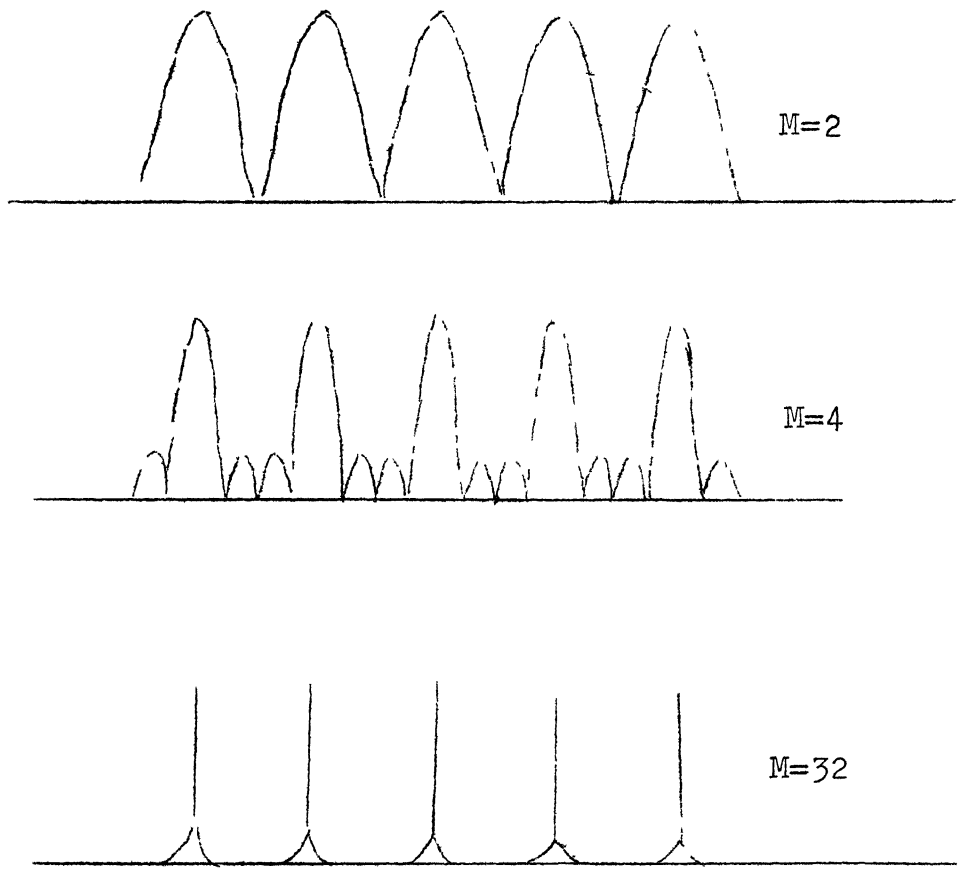

FIG. 2.2 TRANSFER FUNCTION OF A SIGNAL AVERAGING SYSTEM FOR INCREASING NUMBER OF SUMMATIONS.

process, measurements are not possible because the displayed signal grows with each repetition. To enable calibrated real time signal averaging an algorithm called the normalized averaging is also used in all digital signal averagers.

Another algorithm provides SNR improvements for slowly changing signals 'exponentially weighted averaging' gradually de-emphasizes old information with respect to new information to produce a continuous running average of input waveform [7]. This algorithm is also discussed in this section.

Normalized Averaging: The averager samples the input signal f(t) every T seconds, and accumulates in its memory the sample values taken on successive repetitions of the input signal. If the sync pulse marking the beginning of the kth repetition of the signal occurs at t_k, then the average value stored in the ith memory location after K repetitions should be

$$A^i_K = \frac{(K-1)\, A^i_{K-1} + f(t_k + iT)}{K}$$

$$= A^i_{K-1} + \frac{f(t_k + iT) - A^i_{K-1}}{K} \qquad (2.10)$$

where A^i_{K-1} = Average value of the signal stored in the ith location of the memory, after (K-1)-repetitions.

A^{i}_{K} = Average value of the signal, after K repetitions.

$f(t_k+iT)$ = Sampled value of the input signal at the (t_k+iT) instant.

This turns out to be a difficult algorithm to implement because of the large amount of hardware needed for a fast division by K. Implementation of an approximated form of the equation (2.10) results in normalized averaging (pseudo averaging).

In normalized averaging, we approximate equation (2.10) by

$$A^{i}_{K} = A^{1}_{K-1} + \frac{f(t_k+iT) - A^{i}_{K-1}}{2^N} \qquad (2.11)$$

where $2^N \leq K < 2^{N+1}$

This division is easy to implement because dividing a binary number by 2^N is just shifting that number N bits right.

Equations (2.10) and (2.11) both give the same value for the signal portion of the average, the second term in each expression is zero when there is no noise. The only difference is in the averaging of the noise. As we might expect, the efficiency of equation (2.11) is less, for a given number of repetitions we do not get quite so much noise attenuation. However, the loss is surprisingly small - it grows asymptotically to 0.77 dB as K becomes large [7].

Exponential Averaging: It is difficult to monitor slowly varying noisy signals using a strict averaging or summation technique, because the averager's transfer function (the width of the comb filter teeth) changes with each signal repetition.

What is really needed for slowly changing signals is an averaging algorithm that does not change with each repetition. Such an algorithm is

$$A^{i}_{K} = A^{i}_{K-1} + \frac{f(t_k + iT) - A^{i}_{K-1}}{X} \qquad (2.12)$$

$$= \frac{1}{X} \sum_{m=1}^{K} \left(\frac{X-1}{X}\right)^{K-m} f(t_m + iT)$$

where X is a fixed integer, the same for all K.
As X becomes large, the factor $\left(\frac{X-1}{X}\right)^{K-m}$ approaches $e^{-(K-m)/X}$. Hence, this algorithm produces an exponentially weighted average. It can be shown [8], the S/N enhancement for a signal mixed with random noise, using this algorithm approach a factor of $\sqrt{2X}$ as K becomes large.

The implementation of this algorithm is easy, if we select $X(= 2^N)$ as a power of 2. In this method, of averaging, the width of the comb filter's teeth is kept constant, after a preset number of repetitions.

It can be seen by inspection that if N is small, the averaged signal quickly adapts to changes in the input signal.

If N is large, the average responds very slowly to changes in the input signal. The time constant for adapting to changes is approximately 2^N divided by the signal repetition rate. But if N is large, the average also exhibits a much greater S/N improvement.

The exponentially weighted average can be very useful in setting up experiments. Often an improvement of only 3 to 6 dB in S/N is enough to show the experimenter whether any experimental parameters need adjustment, and with this small S/N improvement, the average will follow the adjustments quite rapidly. Thus the experimenter can zero in quickly on the parameters he wants.

In all the digital averagers, using the algorithms described above, the speed with which data or waveforms could be acquired depends on the analog to digital conversion speed and on the memory access time. High resolution, fast analog to digital converters are prohibitively costly. Using a medium speed analog to digital converter, we can achieve not more than 5 μsec resolution perpoint in the digital signal averagers.

If we want to acquire signals having low duty cycle, with resolution as high as 100 nsec, using a medium speed analog to digital converter is not possible. In such situations, signal averagers can be obtained in low cost, but time resolutions as high as 100 nsec by using fast serial analog storage devices.

2.3 CHARGE TRANSFER DEVICES (CTD) FOR HIGH SPEED TRANSIENT ANALOG STORAGE

Charge transfer devices [9] function in the discrete-time domain by storing samples of the input signal in an analog memory as packets of charge. The charge is transferred under the control of a clock to the next storage site. There are two types of these multiple transfer devices, Bucket Bridge Devices (BBD) and Charge Coupled Devices (CCD). The differences between them are primarily in the details of the device structure. The CCD technology is capable of higher sampling rates and higher density devices.

The simplest CCD signal processing device is the serial input, serial output CCD, i.e. the delay line. Although the CCD delay line is a useful device, the complexity of signal processing functions which can be accomplished with CCD's is much greater than time delay. An important feature of the CCD's is that the transfer of analog sample is controlled by digital clock circuits. Since digital circuits can be designed to produce any desired timing sequence, a great amount of design flexibility is inherent in CCD signal processing technology [11, 1,5].

The serial input/serial output structure of CCD's has general applications as a coherent analog delay, as the delay element in recursive filters, and as a variable data rate buffer for time base compression or expansion. These devices can have charge dynamic ranges on the order of

10^4 - 10^5 and delay-bandwidth products of a few thousands.

Using CCD's, time axis conversion may be carried out for blocks of data no greater than the storage capacity of the CCD by using different clock frequencies for the entry and exist of data. A transient recorder may take advantage of the high clock frequencies for data collection followed by a slow readout to the following circuitry.

The key parameter for a CTD is the charge-transfer inefficiency [15]. A small quantity of charge is left behind at each transfer event and eventhough it may be as small as 10^{-5} times the transferred charge, it can cause a significant corruption of a following charge sample after several hundred transfer events. Various techniques are available to enable the effects in a particular application to be minimized [3,4,5,11].

The charge-transfer inefficiency depends upon the clock-frequency. If the clock frequency is continually increased, a point is reached where insufficient time is allowed for all the charge to transfer.

Presently, CCD's with 20 MHz clock rates are available in IC technology. If the analog signals with high bandwidths, are to be acquired with resolutions as high as 100 nsec., CCD's can be used to sample and buffer these signals.

As mentioned in Chapter 1, there is one more major category of discrete time analog signal processing devices besides charge transfer devices. This second category is

Single Transfer Devices (STD). These devices are essentially a set of N parallel integrated sample and holds (see Fig. 2.3).

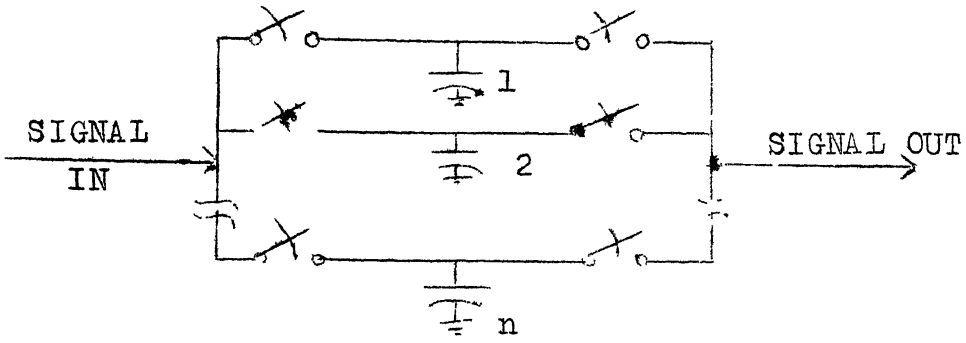

Fig. 2.3: Sample and hold model of STD.

Each successive sample is stored in a separate discrete memory cell, where it stays until it is readout. They do not have the problem of transfer inefficiency of CTD's because of the single transfer. An important feature of these devices is the total independence of the read-in and read-out functions. It is possible to do time base expansion by using different rate clocks for reading-in and reading-out.

Due to the inherent problem of charge-transfer inefficiency in CTD's, STD's give better performance where a temporary buffering of discrete analog samples are needed. In the following section, we will see how a STD can be used for high resolution signal averaging.

2.4 A HIGH-RESOLUTION HYBRID SIGNAL AVERAGER CONFIGURATION

A significant drawback of digital signal averager's is that they cannot acquire signals, with high speed, due to

the limitation in the A/D converter speeds, and in the memory access times. Even when A/D converters with high conversion speeds are available, they are prohibitively costly.

With the advent of charge-transfer devices and single transfer devices, analog signals with high bandwidths can be acquired and temporarily stored as discrete samples. A CTD time-base expander could be used to improve the resolution of the digital signal averager, by receiving the signals with relatively high bandwidths, then clocking out the samples at a much slower rate, so that processing in the digital averagers could take place at a more reasonable speed during the off-period of the signal. Thus, using a CTD time base expander with a digital signal processor results in a low cost high speed hybrid signal averager.

Next chapter, gives the system specifications for the hybrid multi-point averager and discusses the system design considerations.

CHAPTER 3

SYSTEM SPECIFICATIONS AND DESIGN

3.1 SYSTEM SPECIFICATIONS

The following specifications have been laid down for the signal averager, under development, incorporating the hybrid technique for realizing the relatively high time-resolution capability in a cost effective way.

System Configuration:

The system is modular in configuration. It is to have a normal resolution stand-alone main-frame and the systems resolution capability could be improved by adding a high resolution STD based high speed analog storage plug-in printed circuit board. The two resolution modes are switch selectable.

A. Normal-Resolution Main Frame:

Signal input section:

Coupling	: ac or dc.
Input impedance	: greater than 1 Meg-ohm
Bandwidth	: from dc to approximately 50 KHz
Sampling rate	: upto 100 KHz
Input sensitivity	: $\pm$5V input for $\pm$5V full scale output. (External pre-amplifiers required for higher sensitivities).

Signal digitizer section:

Sample and hold: 2 μsec acquisition time, ±5V full scale.

A/D converter : Successive approximation type, 8 bit resolution, 2 μsec conversion time and 2's complement binary output.

Digital memory unit:

1024 word x 20 bit random-access memory.

Memory access time less than 1 μsec.

Signal recovery modes:

Transient signal capture mode.

Signal averaging mode.

Signal averaging modes:

Normalized averaging: Provides continuous calibrated output. Provides upto 24 dB signal-to-noise improvement.

Exponential averaging: Weighting factor front panel selectable.

Summation averaging: Algebraic summation process. Output should be calibrated by a front panel control, after theend of apresent number of sweeps. Sweep number variable upto 4096.Provides upto 36 dB SNR improvement. In this mode word position selector gives scaled memory read-out facility.

Signal output section:

Analog signal output: ±5V corresponding to full scale. Available at a BNC connector.

Digital output: 8 bit, 2's complement binary output.

Synchronizing trigger channel:

Synchronization modes: Internal, External and Manual.

Internal: TTL compatible pulse available at back panel, provides stimulus to the process being monitored.

External: Trigger should be TTL compatible.

Post trigger delay: Variable in steps and continuously in each range from 0.1 μsec to 10 sec.

Time base:

Resolution (per point): 10 μsec to 999 msec in steps of 1 μsec. Number of points selectable from 64 to 1024 as powers of 2.

Sweep number: Upto 4096 sweeps. Selectable from 64 to 4096 as powers of 2.

Sync. output: A 5V positive pulse, approximately 1 μsec wide from a TTL gate. The pulse occurs at the beginning of data read-out and is used to externally synchronize an oscilloscope sweep or other display devices.

System controls:

Start: Initiates data accumulation.

Temporary stop: Stops accumulation at the end of the on-going sweep.

Resume: Resumes data accumulation.

Start read-out: Initiates, repeated availability of processed data, in time sequence to a display device.

D.C. power supplies:

+15V, -15V and 5V derived from 230V, 50 Hz AC mains.

B. High Resolution Analog Storage Unit:

Signal input section:

Input sensitivity : ±5V input

Bandwidth: upto 2 MHz

Analog sampling rate: 0.2 μsec. to 5 μsec. in 5 steps in 1-2-5 sequence.

Signal output section:

Sampled analog read-out rate: approximately 75 KHz fixed synchronized to normal-resolution signal averager section.

3.2 SYSTEM DESIGN

In this section, the system is described at a block schematic level. As mentioned earlier the system is modular in nature. The system consists of a Normal resolution signal averager unit and a Single transfer device (STD) high speed transient analog storage unit as shown in Fig. 3.1.

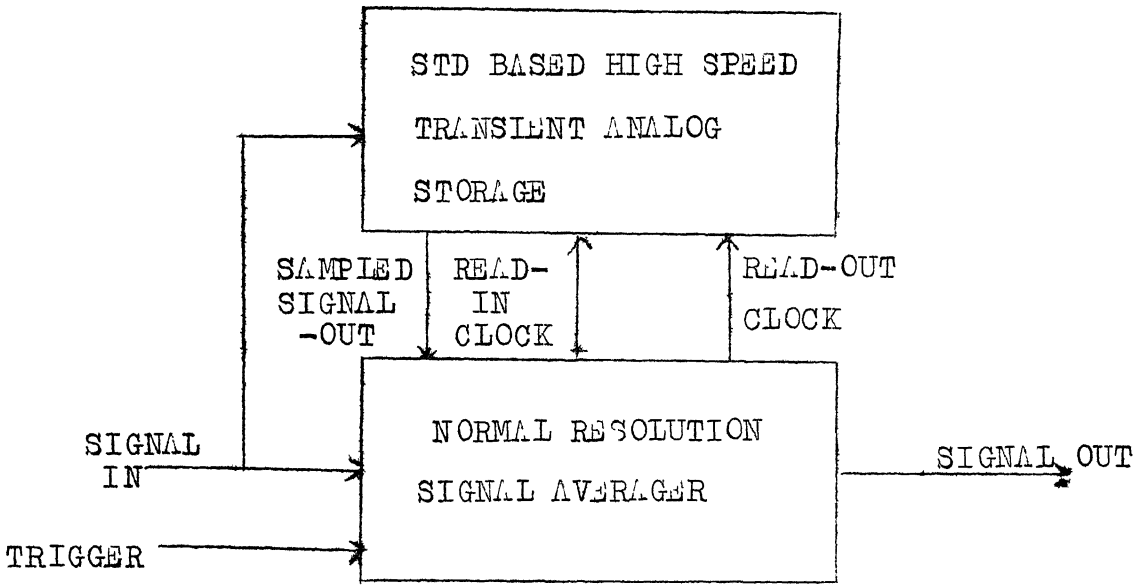

Fig.3.1 Block schematic of a Hybrid Multi-point Signal Averager.

3.2.1 Normal Resolution Signal Averager Design:

A block schematic of the Normal resolution signal averager is given in Fig. 3.2. The normal resolution signal averager, after receiving a synchronizing trigger signal, divides the waveform of interest into finite number of time slots usually referred to as channels and the average corresponding to each channel is computed and stored in a particular location of a memory. The averaging is done by an iterative technique for each channel separately.

The input analog signal, first goes to a sample and hold circuit, where it is sampled and held before it gets converted into a digital form.

As mentioned in Section 3.1, the signal averager performs the three averaging algorithms, (1) Normalized

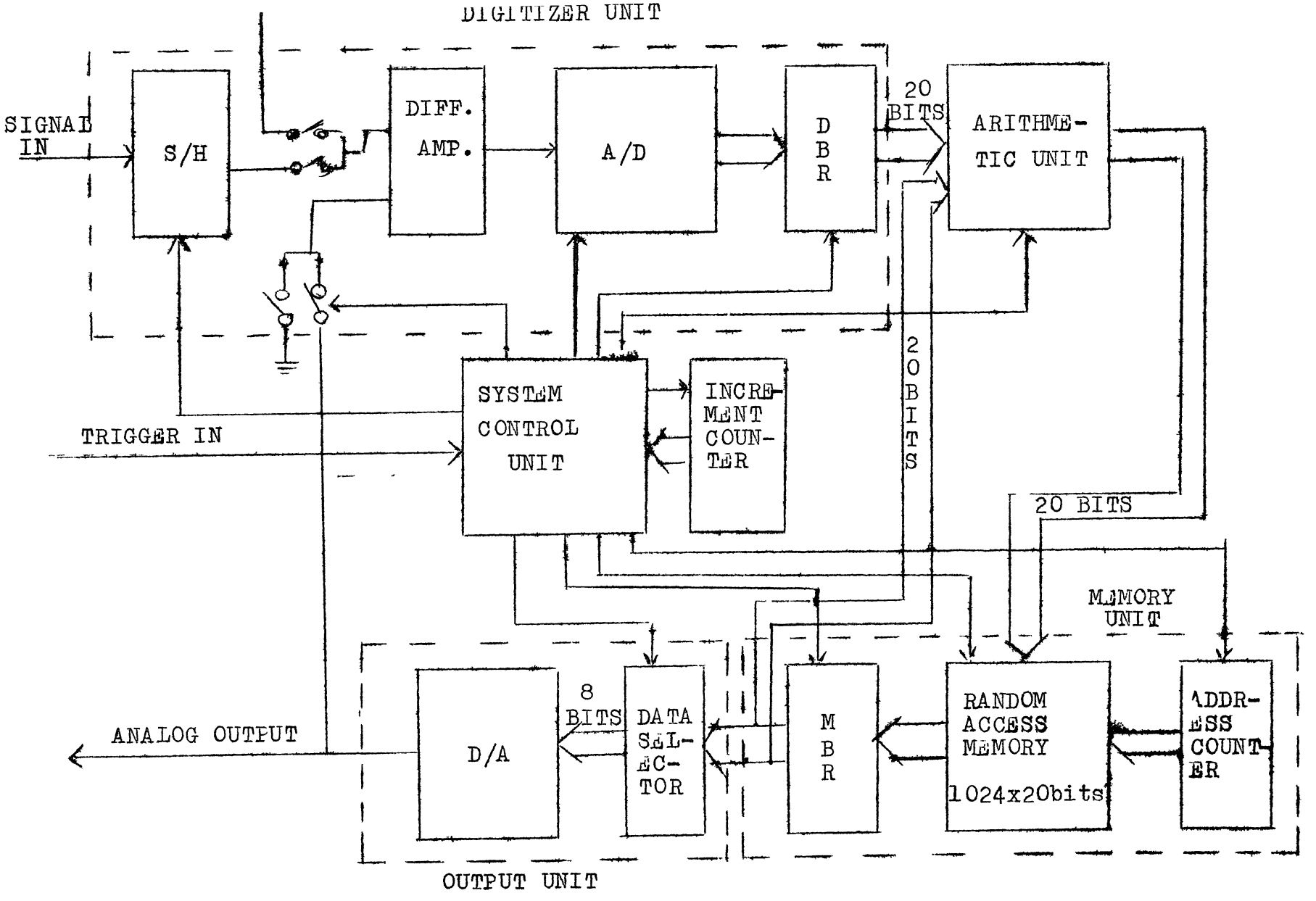

FIG.3.2 NORMAL-RESOLUTION SIGNAL AVERAGER BLOCK SCHEMATIC.

averaging (2) Exponential averaging (3) Summation averaging. For implementing the normalized and exponential averaging algorithms (Equation (2.11) and (2.12)) a subtractor block is necessary in the system. The differential amplifier block in Fig. 3.2, performs this operation. The difference between the input and the old stored average (output of the D/A) is taken before the data is digitized. This means that the A/D converter is looking at the noise, which has an average value of zero. If there are noise spikes large enough to exceed the range of the A/D converter, the resulting round off, or clipping errors will be symmetrical about zero and will not lead to amplitude distortion of the averaged signal.

In the summation averaging, no subtraction is needed. The subtraction operation is inhibited by operating a relay to ground the inverting input of the difference amplifier.

The output of the differential amplifier is digitized by the A/D converter and this digital output is buffered in the data buffer register (DBR). The output is now available at the arithmetic unit.

While performing the summation averaging, the sum grows with each repetition of the signal. The SNIR depends on the number of iterations and this in turn depends upon the word length of the memory. A word length of 20 bits is selected. Using an eight bit resolution A/D,

2^{12} (4096) repetitions of the signal can be averaged without any overflow occurring in the most significant bit. Consistently with the memory word length, the arithmetic unit should have 20 bit input. The output of the A/D is to be converted to a 20 bit word by making all the thirteen MSB's equal to the sign bit of A/D.

The arithmetic unit performs the operations, addition and division. The previously stored average in the memory is available to the adder in digital form. The output of the arithmetic unit is the newly calculated average value. This will be stored in a digital memory. The location of the memory where the new average value will be stored, is generated by an address counter.

The inputs to the arithmetic unit have to be stable when the updated average is being written back into the same location of the previous average value. The memory buffer register is used for this purpose. The necessary control signals for the sample and hold, A/D converter, arithmetic unit and the memory unit are generated by the system control unit.

The trigger, which synchronizes the system, initiates a sweep which increments an increment counter (IC). This IC stores the number (K) of the iteration currently being executed. In the first iteration, MBR is cleared and the data available at the arithmetic unit is written into the memory.

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A data selector block (refer Fig. 3.2) is used to select eight bits out of 20 bits available from the memory. The position of a string of 8 bits can be placed anywhere (8 positions) in the twenty bit memory. When the averaging is in progress only 7 LSB's and the sign bit are selected.

The output of the system is available after converting data selector output to analog form. The averaging ends after a preset number of sweeps (front panel selectable). The contents of the memory can be read-out continuously in a repetitive mode on a CRT display or a strip chart recorder. A sync signal is provided, along with the analog signal, to trigger any external display device used.

3.2.2 STD Based High Speed Analog Storage Unit:

As described in Chapter 2, a cost effective way of achieving high resolution signal averagers is to use a high speed serial analog memory for sampling the analog signals at a faster rate and to store these samples temporarily. After the end of the input sampling, the stored samples can be read-out at a rate compatible with the digital averager.

The block schematic of a high speed analog storage unit is given in Fig.3.3. The building block of this unit is the serial analog memory. The design is based upon the Reticon's serial analog memory chip (SAM-128V). This device time samples an analog input signal and provides first-in, first-out storage for 128 samples. Input can be sampled upto 5 MHz rate. The sampling rate can be increased

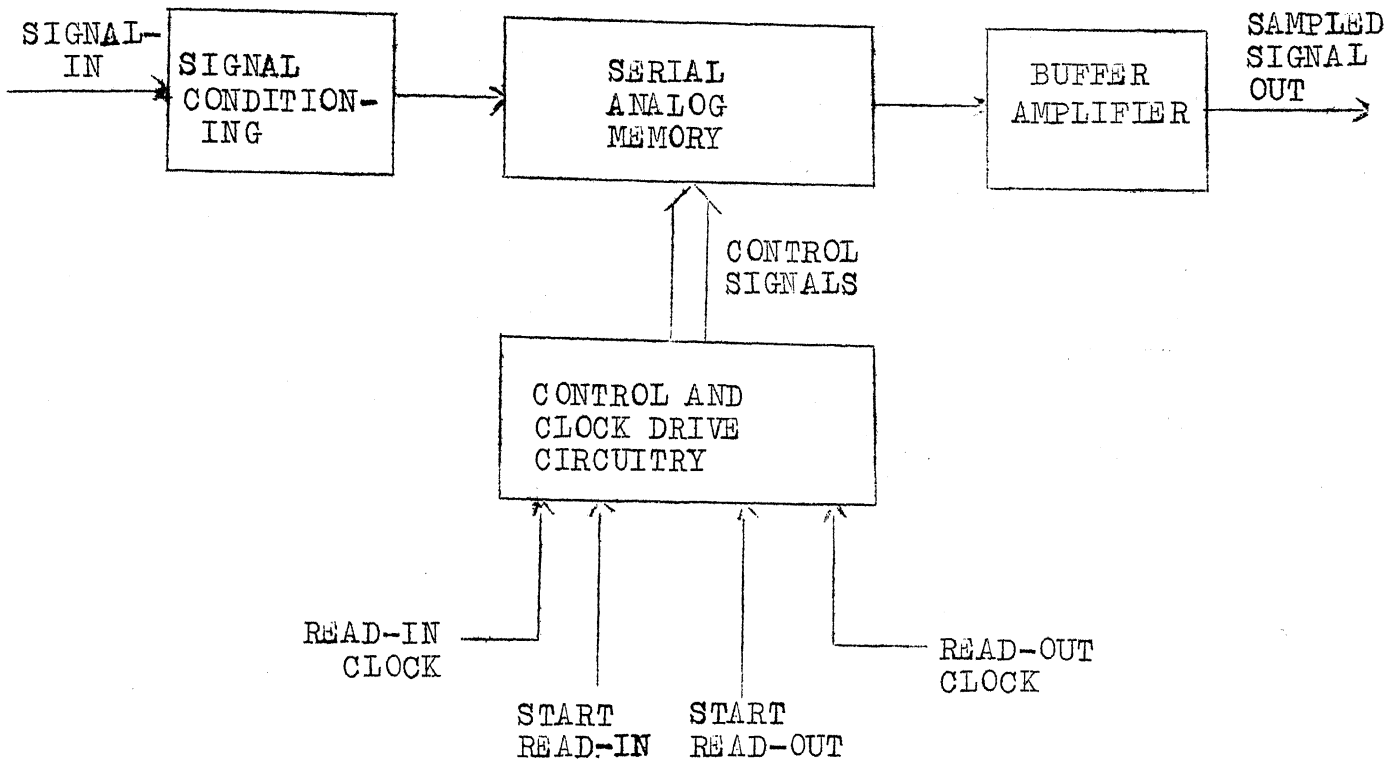

FIG. 3.3 BLOCK SCHEMATIC OF A HIGH SPEED ANALOG STORAGE UNIT.

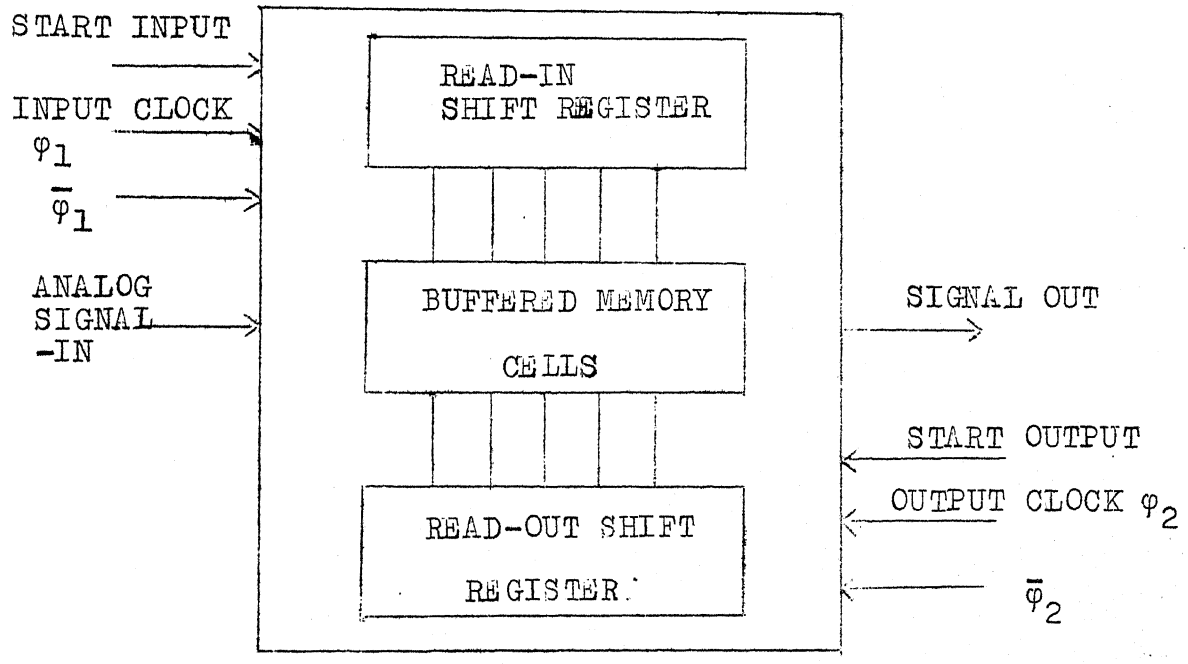

FIG. 3.4 FUNCTIONAL ORGANISATION OF THE SERIAL ANALOG MEMORY.

upto 20 MHz by operating several of these chips in parallel. Read-out is non-destructive and the memory retentivity is upto 40 msec.

The functional organisation of the serial analog memory chip [14], is given in Fig. 3.4.

The chip consists of two independent shift registers, which are used to activate sequentially two corresponding series of multiplex switches. The two shift registers (Read-in, Read-out) are each driven by complementary square-wave clocks which determine the read-in and read-out sampling rates.

The control and clock drive block in Fig. 3.3 generates the complementary clock drives and the start input and start output drives. These controls are generated from the inputs to the control block. The circuit which generates these control signals is described in Section 4.6. The output buffer amplifier is needed to interface the output of the memory to external circuits.

In the following chapter, the system hardware description is presented.

CHAPTER 4

SYSTEM HARDWARE DESCRIPTION

In this chapter, the hardware description of a hybrid signal averager system is presented. In the first five sections, implementation of various blocks in the normal resolution averager are discussed in detail. A section is devoted for the control generation for the serial analog memory. In the last two sections constructional feature and operational details are presented.

The normal-resolution averager comprises of digitizer unit, arithmetic unit, memory unit, system control unit and output unit, as indicated in Fig. 3.2 and these units are described in detail in the following.

4.1 DIGITIZER UNIT

This unit comprises of sample and hold, difference amplifier,analog to digital converter (A/D) and data buffer register (DBR) functional blocks. The timing diagram for various control signals is shown in Fig. 4.1.

4.1.1 Sample and Hold and Differential Amplifier:

A single chip is usedfor the sample and hold function. The acquisition time of the S/H is 5 μsec.,the hold made droop rate for this chip is 50 mV/sec and the control input is TTL compatible.

A high slew rate (35V/μsec) Op-Amp is used to minimize the difference amplifier settling time. The difference between the preset sample and the previously stored average is taken in the analog form.

4.1.2 Analog to Digital Converter and Data Buffer Register:

The output of the difference amplifier is converted into digital form by using an 8-bit successive approximation A/D. The A/D module gives 2's complement output for bipolar signals in the range of ±5V. Once a start convert pulse has been given, A/D gives an end of conversion (EOC) pulse for 2 μsec, indicating that the conversion is going on. At the negative edge of this pulse data becomes valid and at this edge the data is loaded into the data buffer register.

The data buffer register is made of two (74174) chips.

4.1.3 Controls for the Digitizer Unit:

The necessary control signals are S/H control, start convert and load DBR. The S/H control generation is discussed in Section 4.4. The start convert pulse is generated from the S/H control by using two monostables. One monostable is used to provide the necessary delay for the difference amplifier output to settledown to its final value.

From the EOC, load DBR pulse is generated (Refer Fig.4.1). A simplified circuit diagram of this digitizer unit is shown in Fig. 4.2.

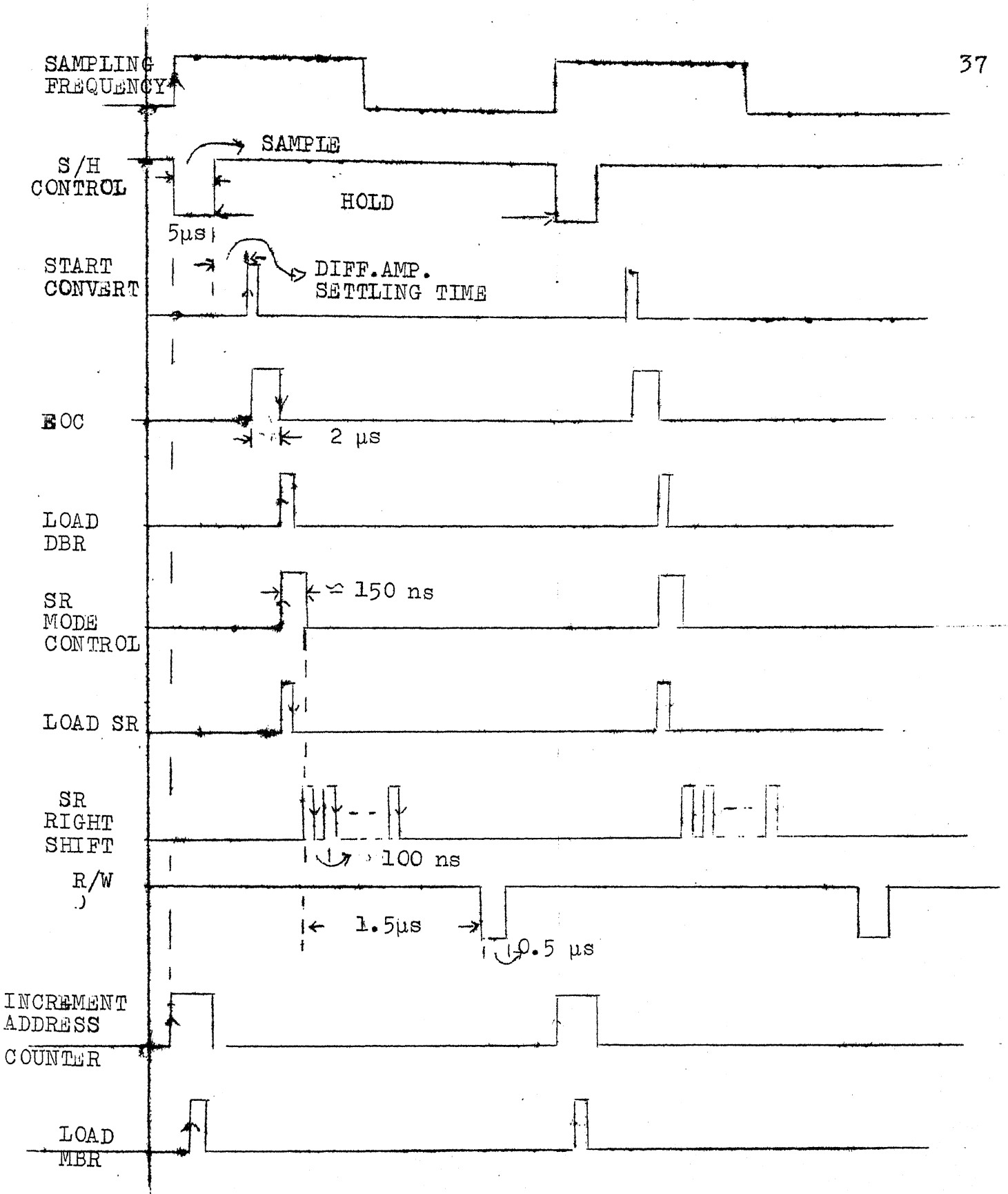

FIG.4.1 TIMING DIAGRAM OF DIGITIZER, ARITHMETIC AND MEMORY UNITS

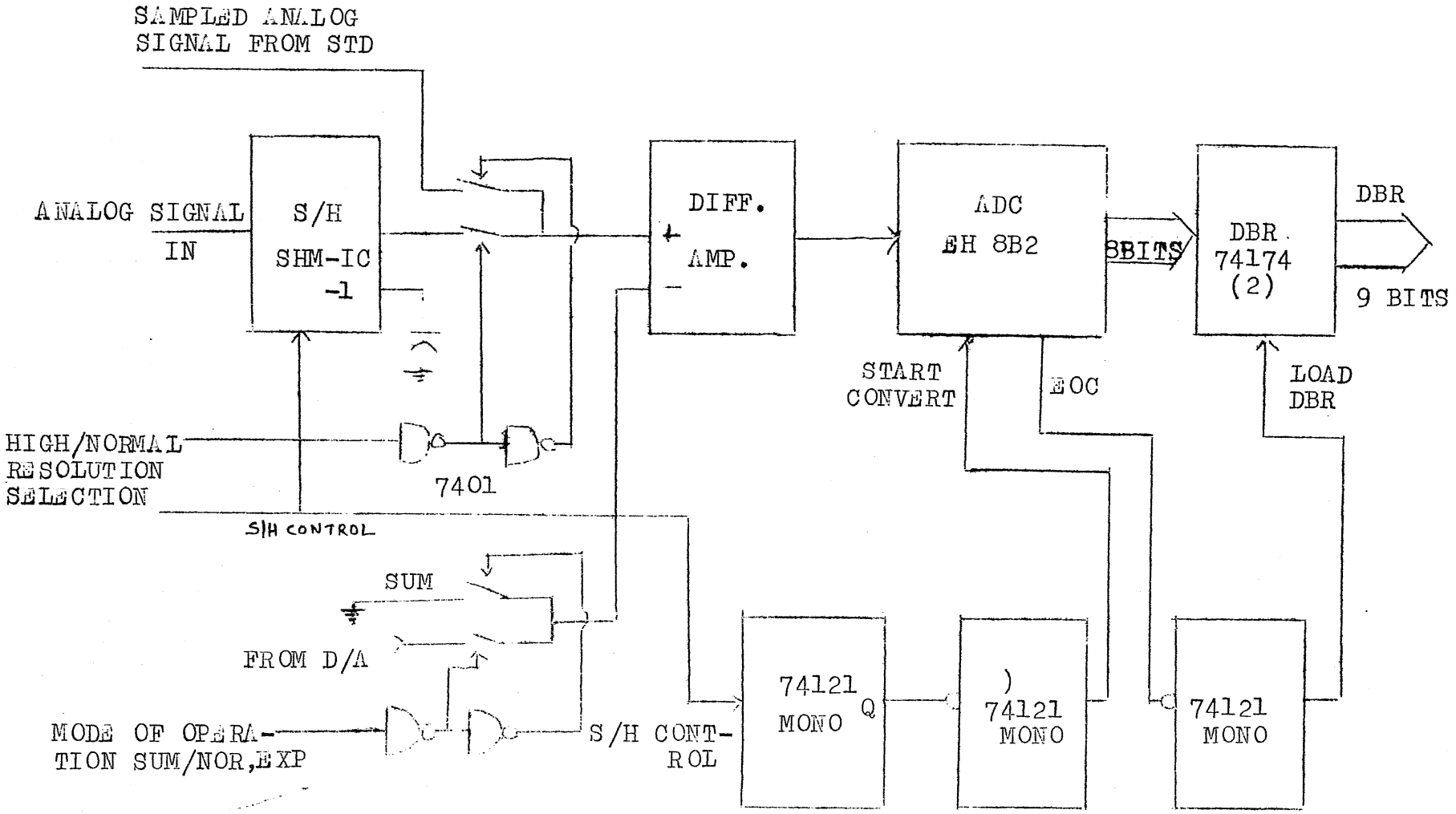

FIG.4.2 A SIMPLIFIED CIRCUIT DIAGRAM OF THE DIGITIZER UNIT.

4.2 ARITHMETIC UNIT

The arithmetic unit consists of a shift register block and an adder block. The shift register block consists of a J-K flip-flop and five 4 bit shift registers. JK flip-flop is used to store the sign bit. Adder block consists of five 4 bit adders.

Simplified block diagram of the arithmetic unit is shown in Fig. 4.3.

We will consider the equations for the three averaging algorithms mentioned in Chapter 2 (Refer equations (2.11) and (2.12)). The algorithm for computing the normalized average is

$$A_K = A_{K-1} + \frac{S_K - A_{K-1}}{2^N} \qquad (4.1)$$

where $2^N \leq K < 2^{N+1}$

A_K = the stored average after K repetitions

A_{K-1} = the stored average after K-1 repetitions.

S_K = the present (Kth) input sample.

Similarly, the algorithm for computing the exponential average is

$$A_K = A_{K-1} + \frac{S_K - A_{K-1}}{2^N} \qquad (4.2)$$

where 2^N is now a front panel selected weighting factor.

The algorithm for computing the summation average is

$$A_K = A_{K-1} + S_K \qquad (4.3)$$

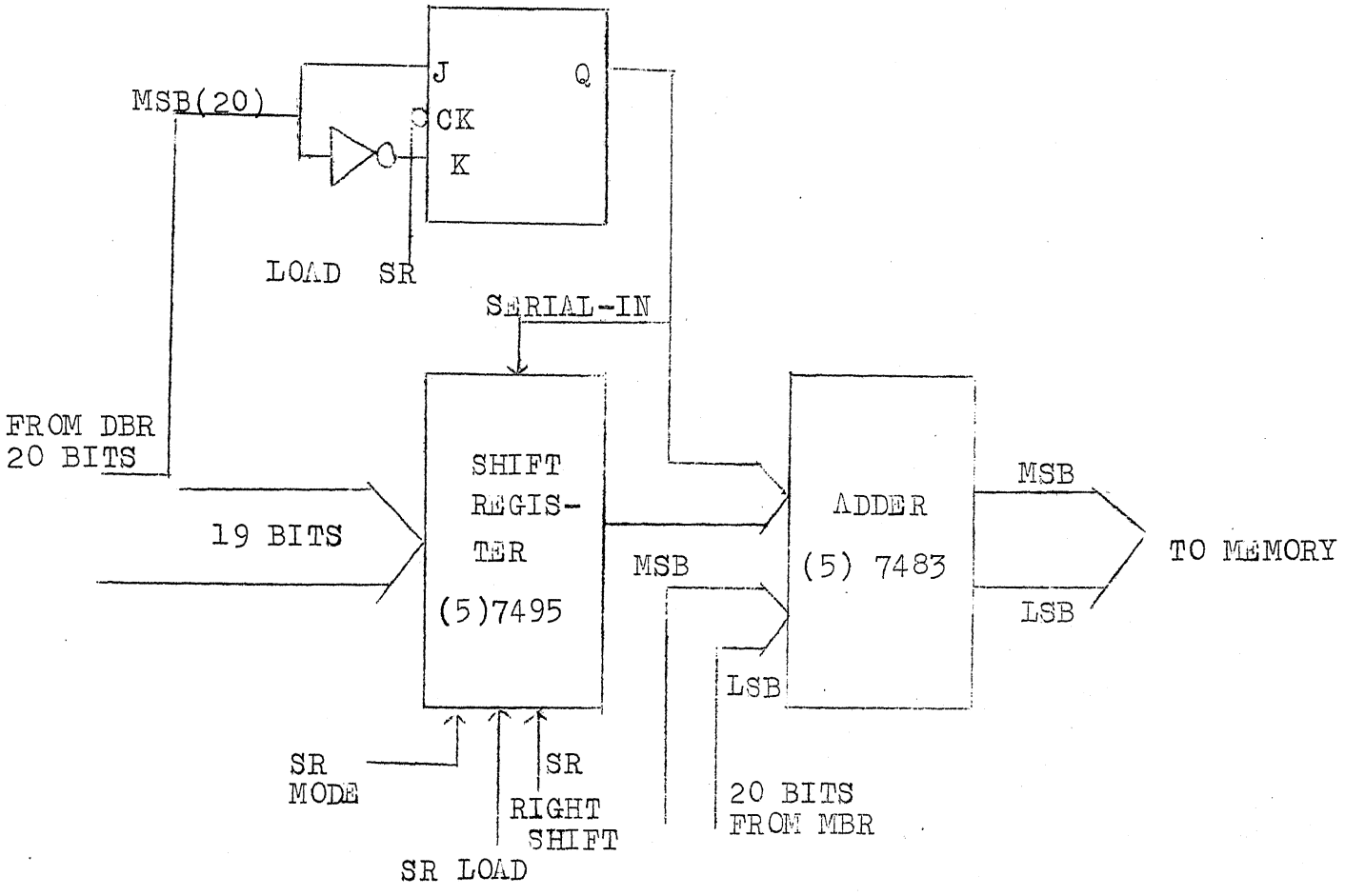

FIG. 4.3 SIMPLIFIED BLOCK DIAGRAM OF THE ARITHMETIC UNIT.

For computing equations (4.1) and (4.2) one subtraction, one division and an addition have to be performed.

The subtraction is done by an differential amplifier (as mentioned earlier).

4.2.1 Division by 2^N:

Dividing a number by 2^N is easily realised by first loading the number into a shift register and then shifting it towards LSB by N bits.

In the normalized averaging the value of N depends upon the current value of K. Increment counter stores the value of K in binary form, whereas, in the exponential averaging N is independent of K.

Depending on the mode of operation, either K (contents of IC) or exponential weighting factor is selected. The selected number is loaded into a shift register by a load SR pulse, to find the position of the most significant '1'. All the output bits except LSB of the SR are ORed and then ANDed with a free running clock (10 MHz) to generate the SR-right shift clock, which is used to right shift the contents of the shift register. When the most significant '1' reaches the LSB, the right shift clock is disabled.

Using the same load SR and right shift clock, the data available at the arithmetic unit is loaded into another SR and then right shifted N times. Thus division by 2^N takes place (Refer Fig. 4.4).

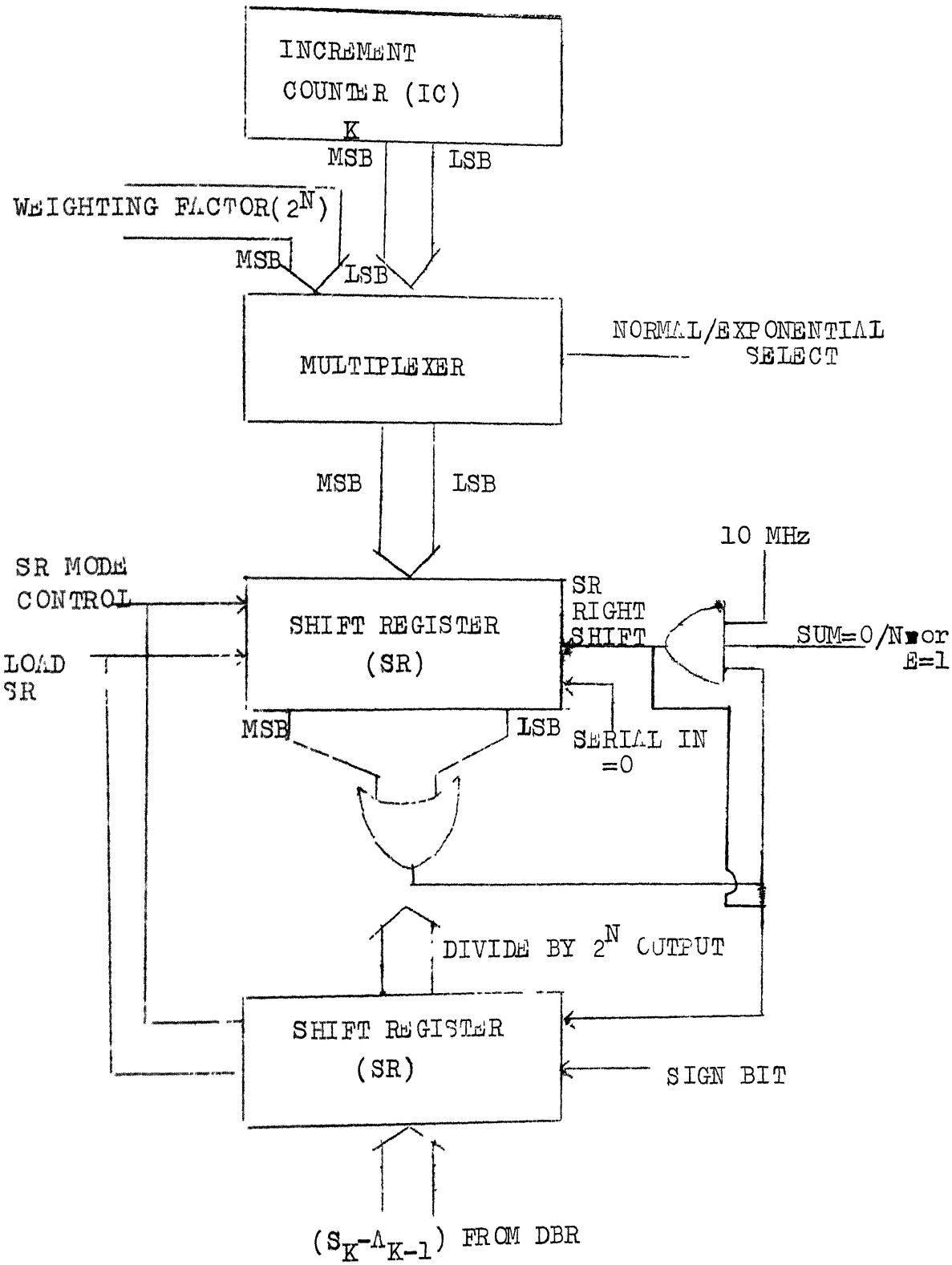

FIG. 4.4 IMPLEMENTATION OF DIVISION.

In the summation averaging,division and subtraction operations are inhibited.

4.2.2 Controls for the Arithmetic Unit:

After the end of the division, the contents of the shift register are added to the contents of the MBR to give the newly calculated average.

The timing for the controls is given in Fig. 4.1. The circuit diagram, generating the control signals for this unit is given in Fig. A.1.2.

4.3 MEMORY UNIT

The memory chip used (12102A-4) is a 1K x 1 bit random access memory. Twenty such chips are used to form a 1024 word x 20 bit memory. The access time of the memory is 450 nsec.

Any location in the memory can be accessed by means of a 10 bit address. The address is generated by an address counter. The address counter is realized by using 3 (74193) synchronous binary counters.

There is a Read/Write (R/W) control for reading from the memory or writing in it. Normally R/W is at logical 1 and the contents of the memory are available for reading. R/W is pulsed to '0' when any data is to be written in the memory.

A memory buffer register is used to store the content of the currently accessed memory location. The clock edge which increments address counter is used to load MBR after a delay of approximately 0.6 μsec. This delay is provided for the memory access time.

MBR is realised using 4 (74174) chips.

4.3.1 Read/Write control circuit:

Approximately 0.5 μsec. should be allowed for addition to be complete, after the end of shifting by K bits and before the newly computed average is written into the memory. Since the maximum number of shifts is 7 (since A/D resolution is only 8 bits), in the worst case R/W should be triggered 0.5 μsec after 7 clock pulses. To ensure this delay clear a 4 bit counter with load SR and start counting up with a free running clock (10 MHz) of the same sequency as SR right shift pulses. This is synchronized with the start of the burst of K pulses. R/W signal is generated when the counter reaches 15 (Refer Fig. 4.1). So we have a delay of atleast 8 clock pulses (= 0.8 μsec.) which is more than our requirement.

The control circuit for the memory unit is shown in Figs. A1.2 and A1.3.

4.4 SYSTEM CONTROL UNIT

System control unit generates control signals required for various units of the system. Detailed system control circuit diagram is shown in Figs. A.1.1, A.1.2 and A.1.3. The timing diagrams are shown in Figs. 4.1 and 4.5.

4.4.1 Sweep Generation:

Sweep is triggered by an external or internal trigger signal. External trigger applied to the system should be TTL compatible. The start of the sweep may be delayed with respect to the trigger instant. The trigger signal is applied to a monostable to obtain the preset delay and the trailing edge of the mono pulse sets a flip-flop. If a sweep triggered by a previous trigger is on, the present trigger is not accepted.

The flip-flop enables a gate to pass the sampling clock which generates the S/H control. The sampling clock is generated from the system clock (10 MHz) by a divider chain and a presettable divider, and this S/H clock increments the address counter. Depending on the number selected (number of points select on the front panel), the rising edge of the particular address line sets a flip-flop. At the end of R/W signal for the sample , address counter is cleared by a sharp pulse and the same pulse also clears the sweep flip-flop (Refer Fig.A.1.3). The sweep, flip-flop output corresponds to the sweep duration and this is used to count the increment counter,

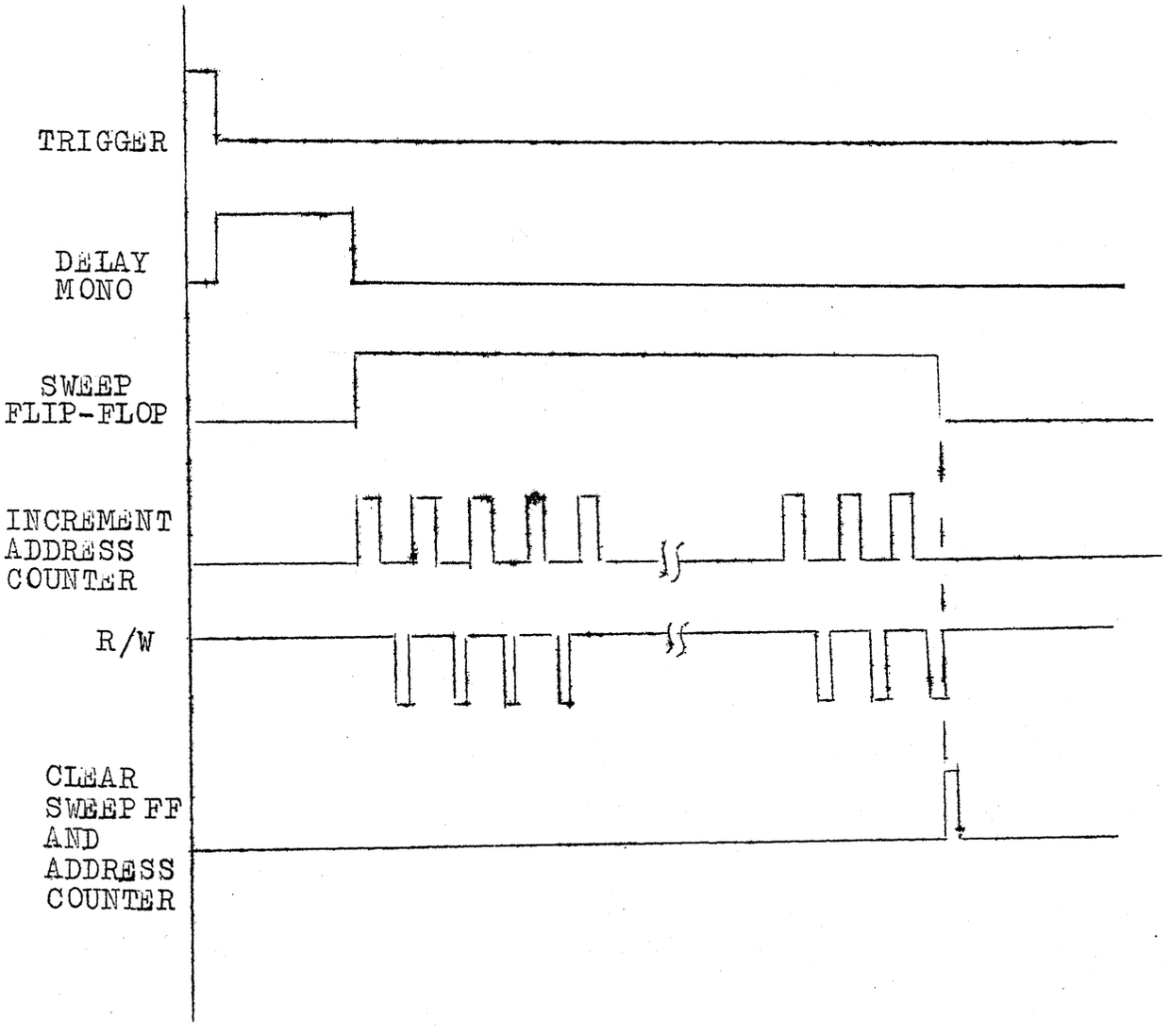

FIG.4.5 SWEEP TIMING DIAGRAM.

which stores the number of iterations currently being executed.

After a preset number of iterations, the trigger to the system is inhibited (Refer Figs. A.1.1 and A1.2). The end of iterations is indicated by a LED. The number of iterations completed is displayed by a 4 digit display on the front panel.

The timing diagram for the sweep generation is shown in Fig.4.5. The control signals required for the various units have been discussed earlier in Sections 4.1 to 4.3.

4.5 OUTPUT UNIT

The output unit comprises of a data selector and a digital to analog converter.

4.5.1 Data Selector and Digital to Analog Converter:

As described earlier in Section 3.1.2, the data selector selects 8 bits out of 20 bits available from memory. The data selector can be used to scale down the contents of the memory in summation averaging.

The data selector is implemented by using 7 eight-to-one multiplexers (74151) chips.

An eight bit D/A converter coaverts digital data into analog form. The D/A accepts 2's complement binary and provides bipolar output with a settling time less than 5 μsec.

4.5.2 Repeated Readout:

The contents of memory have to be read out to an external device for display or print out.

Selection of a particular read mode (CRO, stripchart etc.) enables appropriate clock frequency to be selected. The read out process can be initiated by pressing 'start readout' button on the panel. The selected frequency increments the address counter and also generates the necessary controls for read-out. The timing diagram for repetitive read-out is shown in Fig.4.6.

A sync is provided to synchronize the external display device. The frequency of the sync signal in the CRO mode will be 50 Hz when 1024 points are selected. A flicker free display of the averaged signal can be obtained in this mode.

4.6 CONTROL AND CLOCK DRIVE CIRCUITRY FOR THE SERIAL ANALOG MEMORY (SAM):

In this section, the drive requirements for the serial analog memory are presented and a simplified block diagram is given for generating the control signals for driving the serial analog memory.

Two phase dynamic shift registers are used for both read-in and read-out in SAM [14]. The low power shift register design used in the SAM results in compatibility with CMOS as well as bipolar clock circuits. The proper clock and start waveforms are shown in Fig. 4.7.

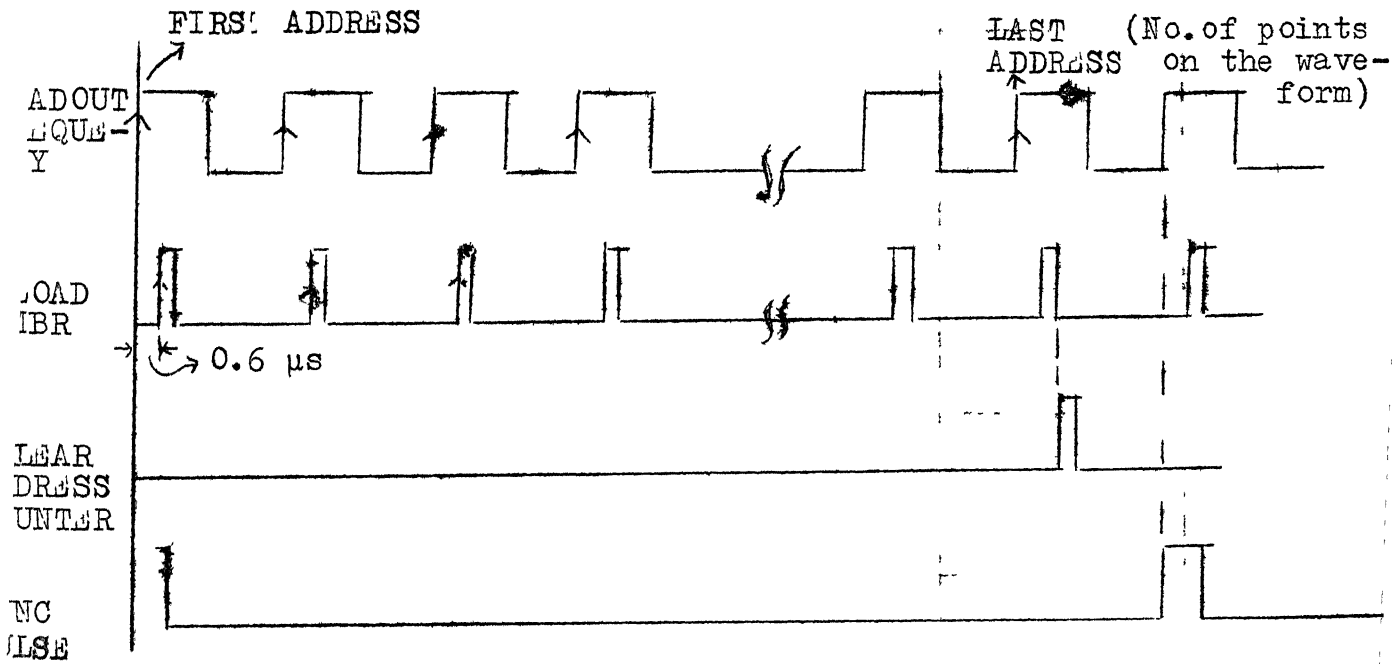

FIG.4.6 TIMING DIAGRAM FOR REPETITIVE READ-OUT.

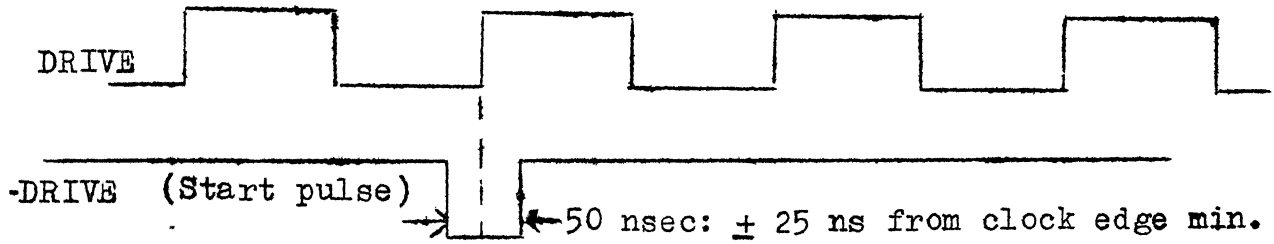

FIG.4.7 TIMING FOR SERIAL ANALOG MEMORY

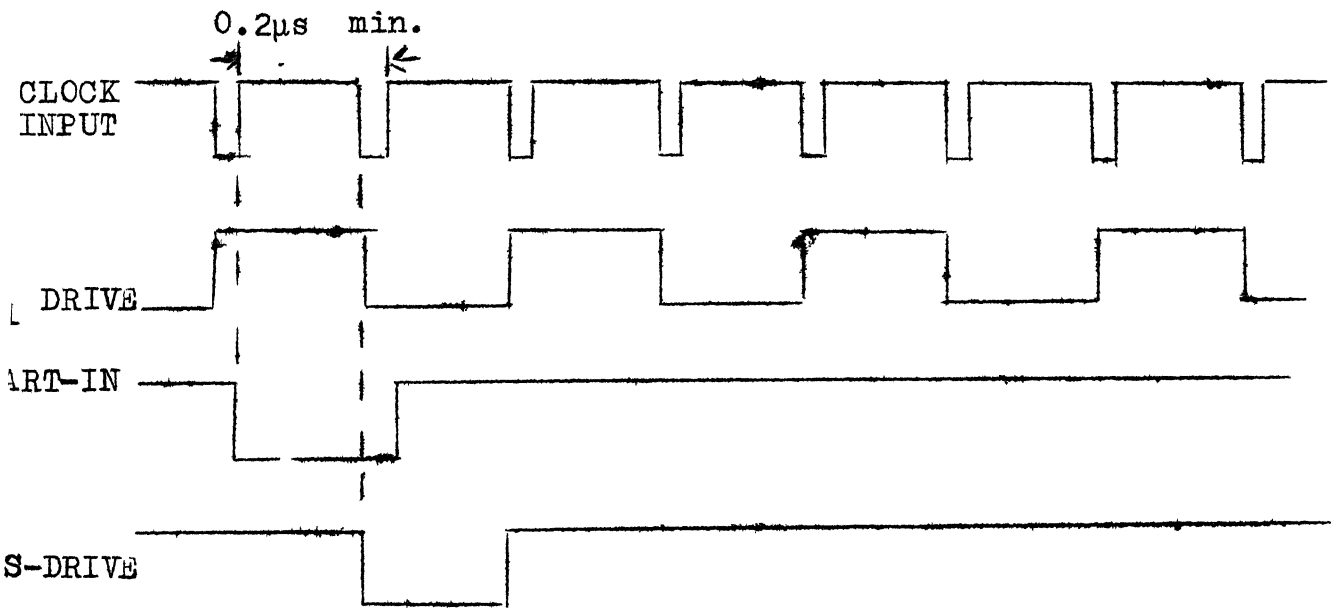

FIG.4.8(A) TIMING DIAGRAM FOR CONTROL AND CLOCK DRIVE CIRCUITRY.

A versatile CMOS circuit capable of generating these waveforms from TTL inputs is shown in simplified form in Fig. 4.8(b) and the timing in Fig.4.8(a). In addition to the two-phase complementary square wave clocks, this circuit generates the periodic start pulses to initiate each read-in and read-out cycle. The circuit of Fig.4.8 ensures the proper timing between the clocks and successively generated start pulses. The proper relationship is of particular importance if one is to obtain uninterrupted linear transformation from input to output.

The critical period for loading a start bit into either register occurs at the negative-to-positive transitions of the φ_1 clock phase. It is therefore necessary that the start pulse be negative for a period of atleast 25 nsec both preceeding and following this transition and it overlap one such transition. In order to sample the input signal or read-out the output signal a new start pulse must be loaded every 128 clock pulses of the appropriate clock.

The circuit of Fig.4.8(b) has some restrictions on the relative timing of the start-in and clock inputs. It is best if the external start input pulses commence coincident with the rising edge of the clock input pulses as shown in Fig. 4.8(a). Then, since the φ_1 drive is synchronous with the falling edge of the clock input, the proper relations are met. Note that an S drive pulse cannot be generated as long as φ_1 is high, but begins as

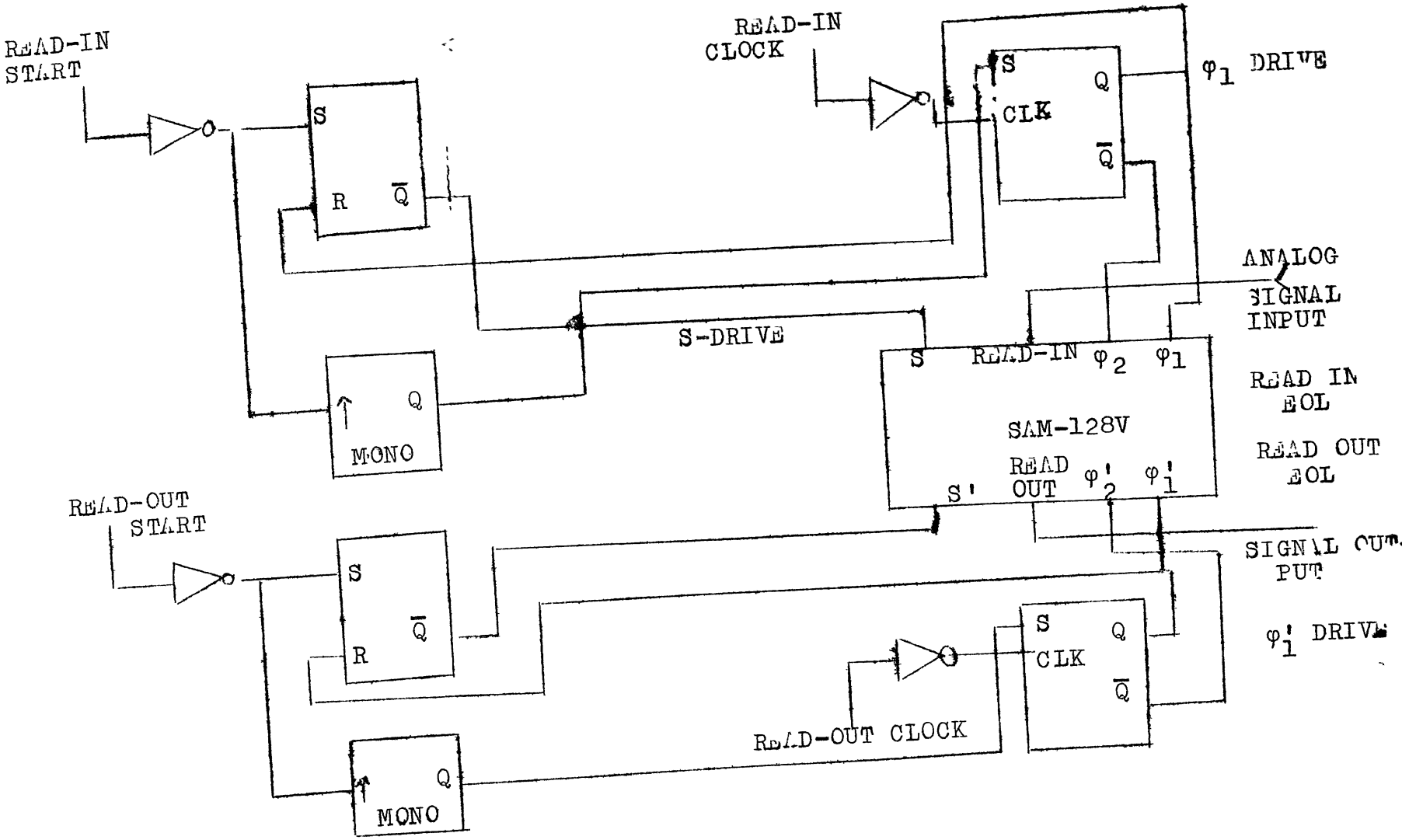

FIG.4.8(B) SIMPLIFIED BLOCK DIAGRAM FOR GENERATING THE CONTROL SIGNALS FOR DRIVING SAM.

soon as φ_1 falls. The start-in pulse must persist long enough following the fall of φ_1 to dominate the control of the S-drive flip-flop.

4.7 PRINTED CIRCUIT BOARDS

The normal resolution signal averager main-frame has been developed. The system circuitry has been distributed over seven printed circuit cards of size 6" x10" . The distribution is as follows:

(1) Input and output - 1 card

(2) Arithmetic unit - 1 card

(3) Memory - 1 card

(4) Memory buffer, data selector and address counter - 1 card

(5) System control - 2 cards

(6) Panel to system interface board - 1 card.

(1) Input and Output Board:

This board contains the following circuits:

(i) Sample and hold

(ii) Difference amplifier

(iii) A/D converter

(iv) Data buffer register

(v) D/A converter

(vi) Sweep generator

(2) Arithmetic Unit Board:

This board contains the following circuits:

(i) Divider

(ii) Adder

soon as φ_1 falls. The start-in pulse must persist long enough following the fall of φ_1 to dominate the control of the S-drive flip-flop.

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This board contains the following circuits:

(i) Sample and hold

(ii) Difference amplifier

(iii) A/D converter

(iv) Data buffer register

(v) D/A converter

(vi) Sweep generator

(2) Arithmetic Unit Board:

This board contains the following circuits:

(i) Divider

(ii) Adder

(3) Memory Board:

This board contains 1024 x 20 bit memory.

(4) Memory Buffer, Data Selector and Address Counter Board:

This board contains the following circuits.

(i) Memory buffer register

(ii) Data selector multiplexers

(iii) Address counters

(5) System Control Boards:

(a) The control card-1 consists of the following circuits:

(i) Increment counter

(ii) Divider control circuit

(iii) System clock

(iv) Read/Write control.

(b) The Control Card-2 consists of the following circuits:

(i) Frequency divider chain

(ii) Address counter and memory buffer control

(iii) Sync generator.

(6) Panel to System Interface Board:

This board contains the necessary gates to encode the panel information. Resistors belonging to the various switches on the front panel have been mounted on this card.

4.8 FRONT PANEL CONTROLS/INDICATORS

The normal resolution signal averager has the following controls and indicators:

1. Mode of operation select
2. Resolution per point select
3. Points on the waveform select
4. Preset number of sweeps select
5. Sweep ready indicator
6. End of preset sweeps indicator
7. Word position selector
8. Read mode selector
9. Start analysis microswitch
10. Temporary stop microswitch
11. Resume microswitch
12. Start readout microswitch
13. 4 digit LED display for sweeps completed
14. Address select manual or auto.
15. Manual pulse microswitch.

4.9 OPERATING INSTRUCTIONS

In order to use the normal resolution signal averager for extracting signals burried in noise, the following operating procedures may be followed:

1. The power switch is turned ON - no warm up is required.
2. Select per point resolution depending upon the resolution required.

3. Mode of operation switch setting.

(i) In the TR mode transient waveforms can be recorded.

(ii) SUM mode performs summation averaging upto the preset number of sweeps.

(iii) Normalized averaging can be selected by selecting the NOR mode. In this mode averaged output is monitored when the averaging is in progress.

(iv) In the EXP (exponential) averaging mode the weighting factor is selected by the setting of the switch. In this mode also output is monitored while the averaging is in progress.

4. No. of points setting depends on the no. of points to be taken on a single sweep.

5. S/N improvement ratio depends upon the no. of sweeps averaged.

6. Start analysis command, starts the averaging or transient reading process and continuous till the end of preset no. of selected.

7. The 'start readout' command monitors the contents of the memory without further averaging.

8. When the averaging is in progress, averaging process can be stopped immediately after the end of the on-going sweep and the contents of the memory can be monitored by the "start readout" command.

9 The averaging process can be again initiated by the 'resume' command.

10 Read mode setting depends upon the external read-out or

CHAPTER 5

CONCLUSIONS

The thesis described the design and implementation of a hybrid multi-point signal averager. The system was configured with available resources in time bound atmosphere, with the result many desirable features had to be left out. some suggestion for improving the system capabilities are discussed below.

(a) As mentioned in Chapter 4, only Normal resolution signal averager has been developed. The resolution of this can be improved by adding a single transfer device (STD) transient analog storage unit With this unit, the resolution achievable is upto 100 nsec.

(b) The signal to noise ratio improvement achievable with the normal resolution signal averager designed is only 36 dB. This is mainly limited by the word length used in the mamory. A higher SNIR (48 dB) can be obtained, with the existing A/D, by increasing the word length to 24 bits.

(c) An amplitude cursor for digital readout of the actual magnitude of a point on the waveform stored will be quite useful, while taking the measurements. This amplitude cursor can also be incorporated in the system by providing a display for amplitude readout and a signal

for illuminating the point on the waveform, which is selected.

(d) A digitally controlled post trigger delay capability will be useful for recovering a segment of interest in the waveform. This facility can also be incorporated in the system.

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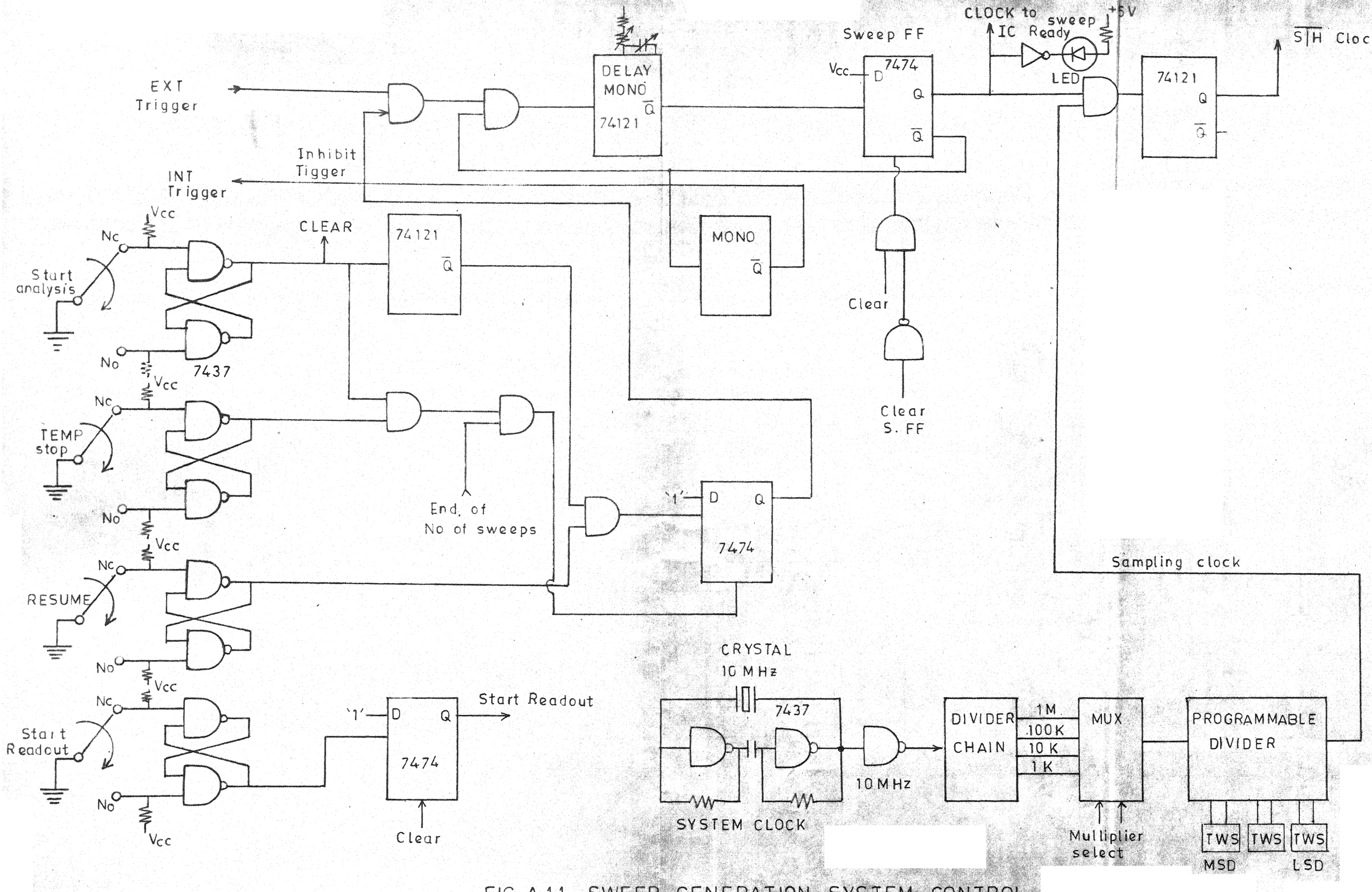

FIG. A.1.1 SWEEP GENERATION-SYSTEM CONTROL

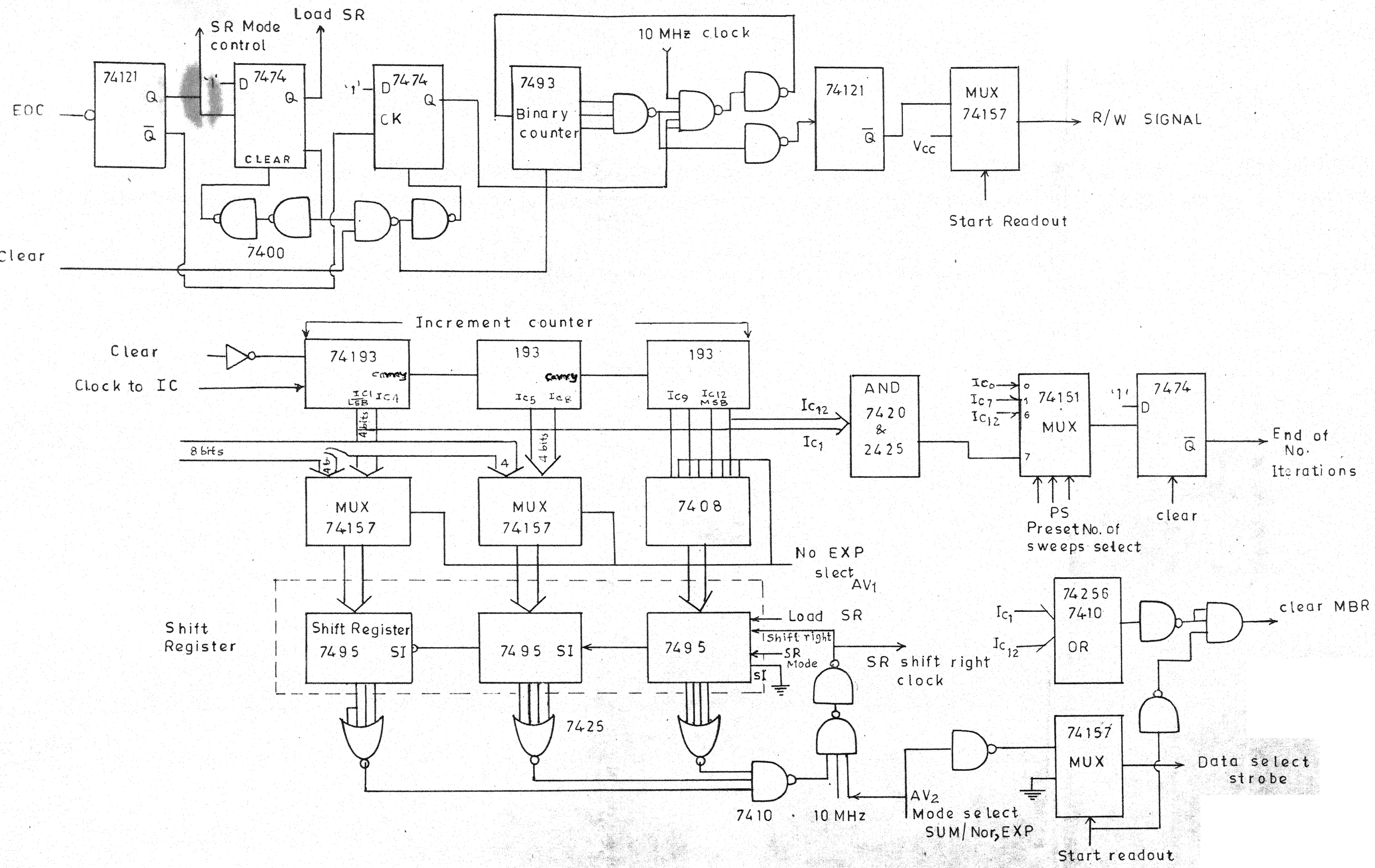

FIG. A.1.2 SYSTEM CONTROL–ARITHMETIC UNIT AND MEMORY UNIT

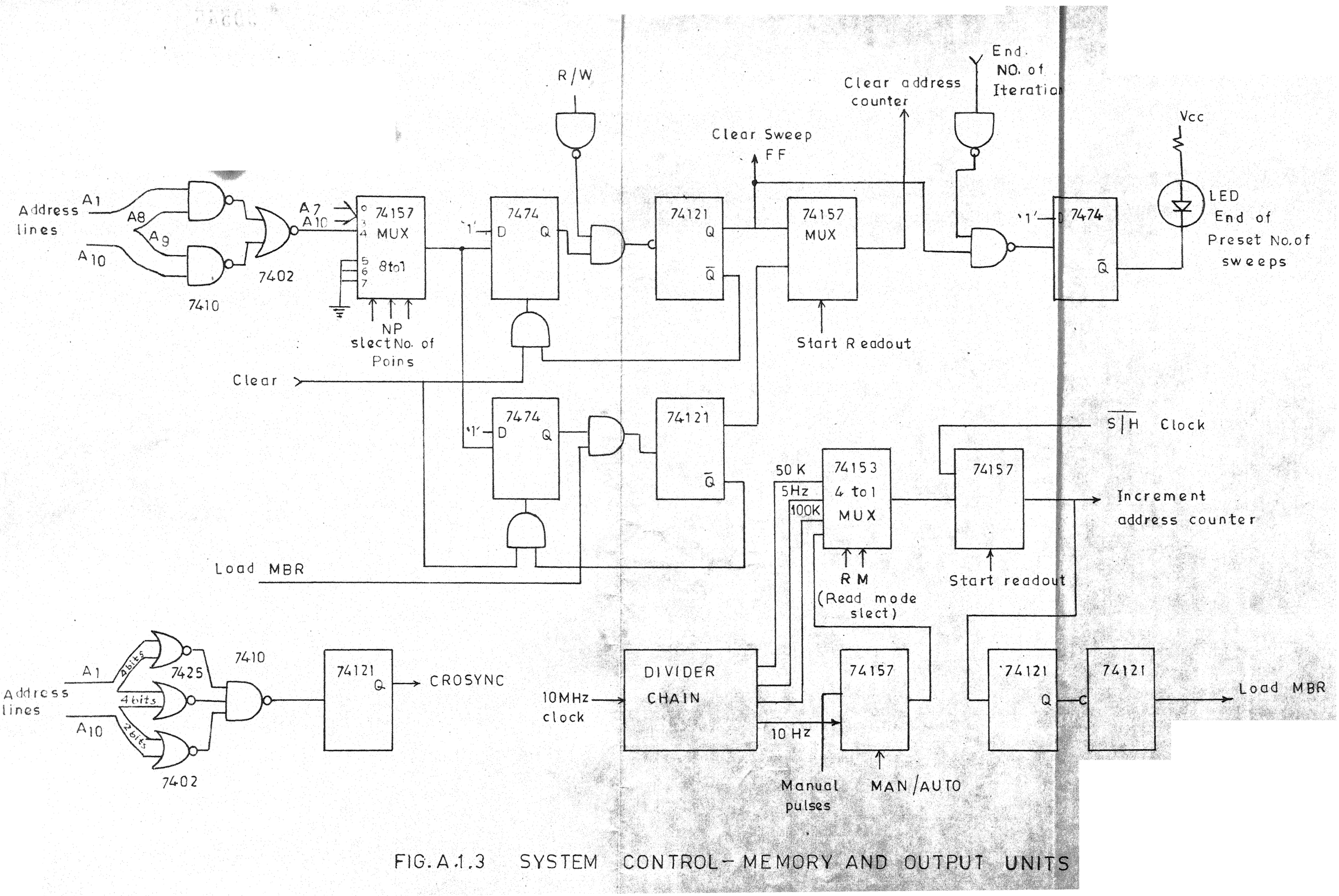

FIG. A.1.3 SYSTEM CONTROL – MEMORY AND OUTPUT UNITS